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CLAIMS 09/575,562

1. A DAC comprising:

a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, at least two of the plurality of sub DACs sharing charge with one another, and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

2. The DAC of claim 1, wherein the multi-bit digital signal is an equally weighted multi-bit digital signal, and the associated amount of charge is the same for each of the plurality of sub DACs

3. The DAC of claim 1, wherein the multi-bit digital signal is an equally weighted multi-bit digital signal, and the associated capacitance is the same for each of the plurality of sub DACs.

4 The DAC of claim 1, wherein each of the plurality of sub DACs shares charge with one another, and the switched capacitor network outputs an analog signal indicative of a sum of values of each bit in the multi-bit signal.

5. The DAC of claim 1, wherein there is a one to one relationship between a number of capacitors and a number of bits.

6. The DAC of claim 1, wherein at least a portion of the plurality of switched capacitor cells form a closed loop.

7. The DAC of claim 1, wherein at least two of the plurality of switched capacitor cells has a orientation direction, and the orientation direction of at least one of the plurality of switched capacitor cells is rotated substantially ninety degrees relative to at least one other of the at least one of the plurality of switched capacitor cells.

8. The DAC of claim 1, wherein each of at least four of the plurality of switched capacitor cells have a orientation direction, and the orientation direction of each of the at least four of the plurality of switched capacitor cells has an angular offset relative to the others of the at least four of the plurality of switched capacitor cells .

9. A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally weighted values of each bit in the multi-bit signal.

10. The DAC of claim 9, wherein the one or more analog signals comprises exactly one signal.

11. The DAC of claim 9, wherein the one or more analog signals comprises two or more analog signals, wherein at least two of the two or more analog signals comprises a single packet of charge indicative of a sum of equally weighted values of each bit in the multi-bit signal.

12 A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally weighted values of each bit in the multi-bit signal.

13. The DAC of claim 12, wherein there is a one to one relationship between a number of capacitors and a number of bits.

14. The DAC of claim 12, wherein at least a portion of the plurality of switched capacitor cells form a closed loop.

15. The DAC of claim 12, wherein at least two of the plurality of switched capacitor cells has a orientation direction, and the orientation direction of at least one of the plurality of switched capacitor cells is rotated substantially ninety degrees relative to at least one other of the at least one of the plurality of switched capacitor cells.

16. The DAC of claim 12, wherein each of at least four of the plurality of switched capacitor cells have a orientation direction, and the orientation direction of each of the at least four of the plurality of switched capacitor cells has an angular offset relative to the others of the at least four of the plurality of switched capacitor cells .

17. A method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising the steps of:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; and

connecting at least two of the plurality of capacitors to one another to share charge with one another.

18. The method of claim 17, wherein the method further comprises connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

19. The method of claim 17, wherein the method further comprises connecting all of the capacitors together so each has substantially the same value.

20. The method of claim 19, wherein each of the capacitors has substantially the same charge.

21. A method of converting a equally weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising the steps of:

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charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal , and

generating a single packet of charge on at least one capacitor indicative of a sum of equally weighted values of each bit in the multi-bit signal .

22. The method of claim 21, wherein the method further comprises connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

23. The method of claim 21, wherein the method further comprises charging each to a level indicative of a value of correspondence and connecting all together so each has same charge.

Sub A8

24. A method of converting an equally weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising the steps of:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal , and

connecting at least two of the plurality of capacitors to one another to share charge with one another.

25. The method of claim 24, wherein the method further comprises connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

26. The method of claim 24, wherein the method further comprises charging each to a level indicative of a value of correspondence and connecting all together so each has same charge.

Sub A9

27. A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; and

means for connecting at least two of the plurality of capacitors to one another to share charge with one another.

28. The DAC of claim 27, wherein the DAC further comprises means for connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

29. The DAC of claim 27, wherein the DAC further comprises means for connecting all of the capacitors together so each has substantially the same value.

30. The DAC of claim 29, wherein each of the capacitors has substantially the same charge.

31. A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal , and

means for generating a single packet of charge on at least one capacitor indicative of a sum of equally weighted values of each bit in the multi-bit signal .

32. The DAC of claim 31, further comprising means for connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

33. The DAC of claim 31 further comprising means for charging each to a level indicative of a value of correspondence and connecting all together so each has same charge.

34. A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal , and

means for connecting at least two of the plurality of capacitors to one another to share charge with one another.

35. The DAC of claim 34, further comprising means for connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

36. The DAC of claim 34 further comprising means for charging each to a level indicative of a value of correspondence and connecting all together so each has same charge.

Sub A12

37. An integrated circuit comprising:

an integrated a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, at least two of the plurality of sub DACs sharing charge with one another, and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

38. An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally weighted values of each bit in the multi-bit signal.

39 An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally weighted values of each bit in the multi-bit signal.

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